REMARKS

Claims 2, 5, 7-10, 15, 18, 20-22, 27-41 and 44-50 are pending in this application, of which claims 27-33 and 39-41 have been withdrawn from consideration and claim 34 has been amended. No new claims have been added.

Claims 2, 5, 7-9, 15, 18, 20-22 and 34-36 stand rejected under 35 USC §103(a) as unpatentable over **Hiroshi** in view of **Atsushi**, both previous cited.

Applicants respectfully traverse this rejection.

As noted in Applicants' response of April 5, **Hiroshi** discloses an integrated circuit device in which a through-hole 11a is provided through an insulating substrate 11, and a wiring board 10 is formed which includes a conductor exposed portion 12b on the opposite surface of an external connection terminal surface 12a of a conductor 12a. Then, an integrated circuit element 13 is mounted on the wiring board 10 at a predetermined position of the same opposite to the conductor 12 of the insulating substrate 11 through a connection member 14 comprising insulative resin, and an adhesive material 14 is heated and hardened for adhesion and fixation of the insulated circuit element. Further, there is performed electrical connection required for an input/output electrode 13a of the integrated circuit elements 13a and the conductor exposed portion 12b of the wiring board 10. Thereafter the integrated circuit element 13, a metal wire 15, and the one surface of the insulating substrate 11 are covered with sealing resin 16 for protection thereof.

It should be noted that conductor 12, corresponding to the metallic film of the present invention, covers only the bottom surface of the resin projection. This is in contrast to the present invention, shown, for example, in Fig. 32, in which the films 113 cover both the bottom and side

surfaces of the resin projections.

The Examiner has applied **Atsushi** for teaching this feature.

Applicants respectfully disagree. Although **Atsushi** discloses an optical semiconductor device in which connecting parts 6 projecting from the resin portion are completely covered by conductor pattern 2, there would be no motivation to apply this teaching to **Hiroshi** because conductor 12 is a flat plate covering the bottom of sealing resin 16 and the wiring board 10. There is no "projection" in **Hiroshi**, only the flat plate. Thus, these references may not be combined to teach the present invention.

Furthermore, with regard to claims 15 and 20-22, Applicants submit that the recited feature of "said resin projections extending downwards from the mount-surface and laterally extending from at least one of the resin package" is not disclosed in **Hiroshi**.

Hiroshi fails to teach the feature of resin projection projecting from the bottom surface of the device. What is disclosed in **Hiroshi** is a resin part projecting from the bottom surface of the chip, but this resin part of **Hiroshi** does not project from the bottom surface of the device. The device of **Hiroshi** has a flat surface.

Atsushi merely teaches a semiconductor chip mounted in a depression formed on a resin body. Thus, the invention of **Atsushi** is inherently different from the invention of the present invention in which a resin sealing is provided after the mounting of the chip.

In regard to claim 10, **Hiroshi** discloses that connection member 14 comprising "insulative" resin. Applicants submit that this material is not the same as "resin tape."

Accordingly, claim 34 has been amended to recite "resin" tape.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 37-38 and 44-50 stand rejected under 35 USC §103(a) as unpatentable over **Hiroshi** and **Atsushi** and further in view of **Hosomi et al.** (previously cited).

Applicants respectfully traverse this rejection.

Hosomi et al. has been cited for teaching the formation of metallic films 3 comprising a plurality of stacked metallic layers but, like **Hiroshi** discussed above, fails to teach, mention or suggest the electrode forming a flush surface with the package body, as recited in claim 34, from which claims 37-38 depend.

Furthermore, neither of the applied references teaches, mentions or suggests that metallic films are provided on bottom and side surfaces of the resin projections, as in the present invention.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/442,038

IN THE CLAIMS:

Please amend claim 34 as follows:

34. (Amended) A device comprising:

a chip;

a resin package sealing said chip, said resin package having a mount-side surface of the resin package which comprises a resin tape;

metallic films respectively provided in the resin package so that the metallic films are flush with the mount-side surface and are exposed therefrom; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.